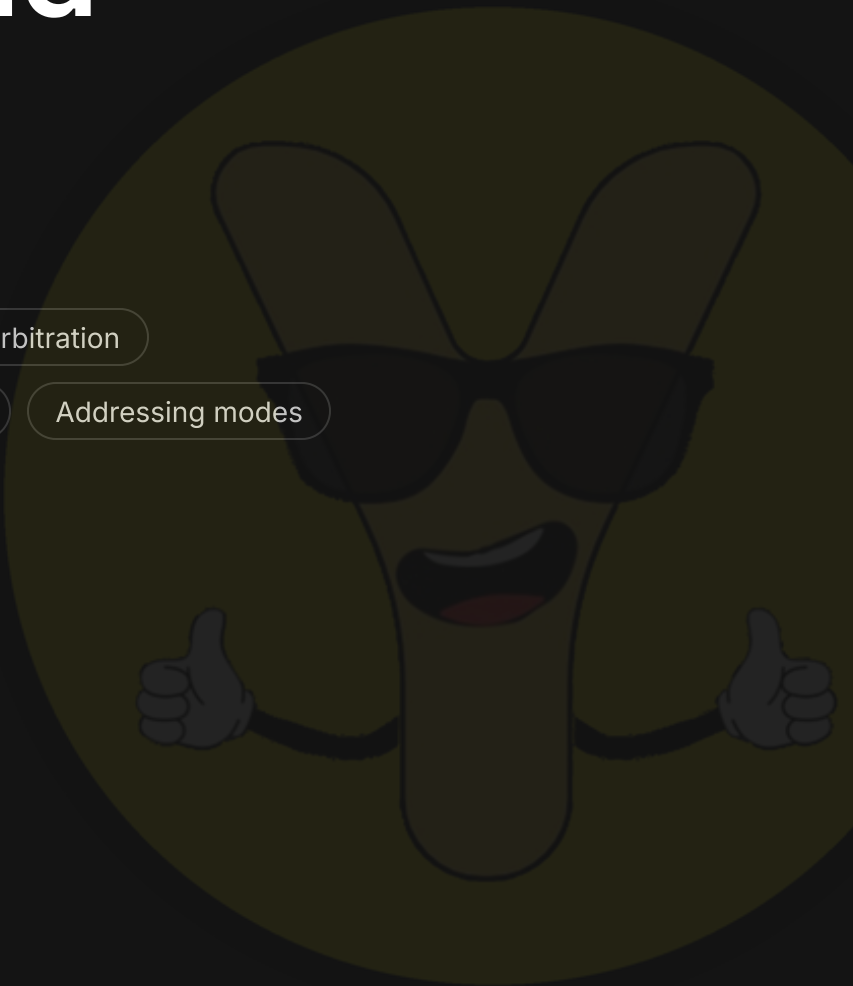
AKTU · 2ND YEAR · SEMESTER 3 · BCS302

Computer Organization and Architecture

Unit 1 — Introduction and Processor Organization

- Functional units of digital system and their interconnections
- Buses, bus architecture, types of buses and bus arbitration
- Register, bus and memory transfer
- Processor organization, general registers organization, stack organization
- Addressing modes



DECODED BY

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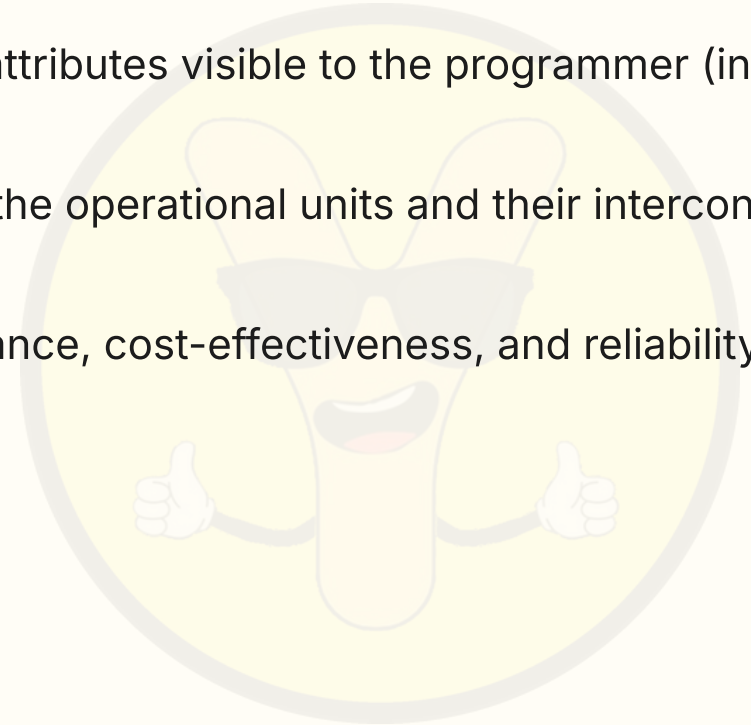
Founder, Ycotes · Gold Medalist in Artificial Intelligence, IIT Madras · taught 10,000+ students

Introduction to Computer Organization

Understanding the foundational concepts of computer architecture and hardware design.

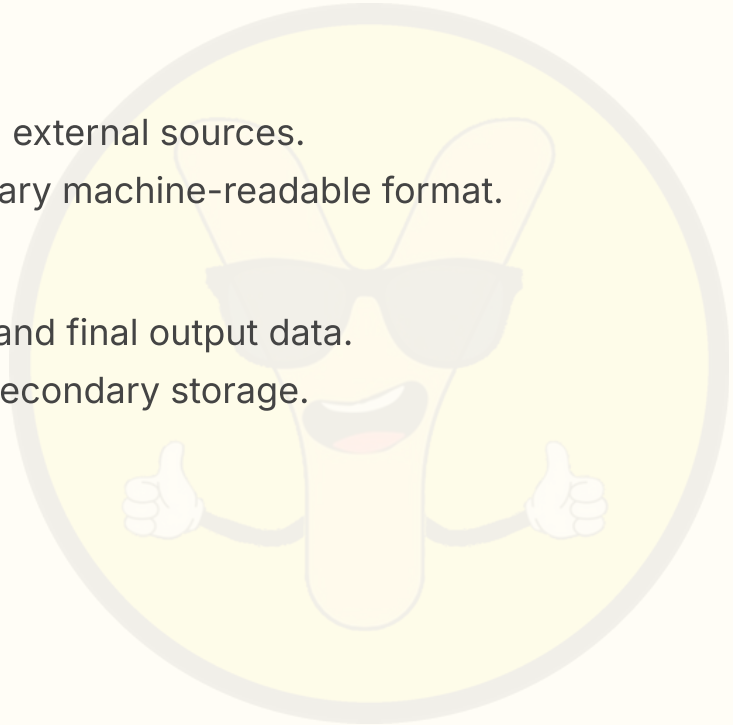
- Computer Architecture deals with attributes visible to the programmer (instruction set, data types, I/O mechanisms).
- Computer Organization deals with the operational units and their interconnections realizing the architectural specifications.
- Goal is to achieve optimal performance, cost-effectiveness, and reliability in digital computing systems.



Functional Units of a Digital System

A digital computer consists of five principal functional units working in synchronization.

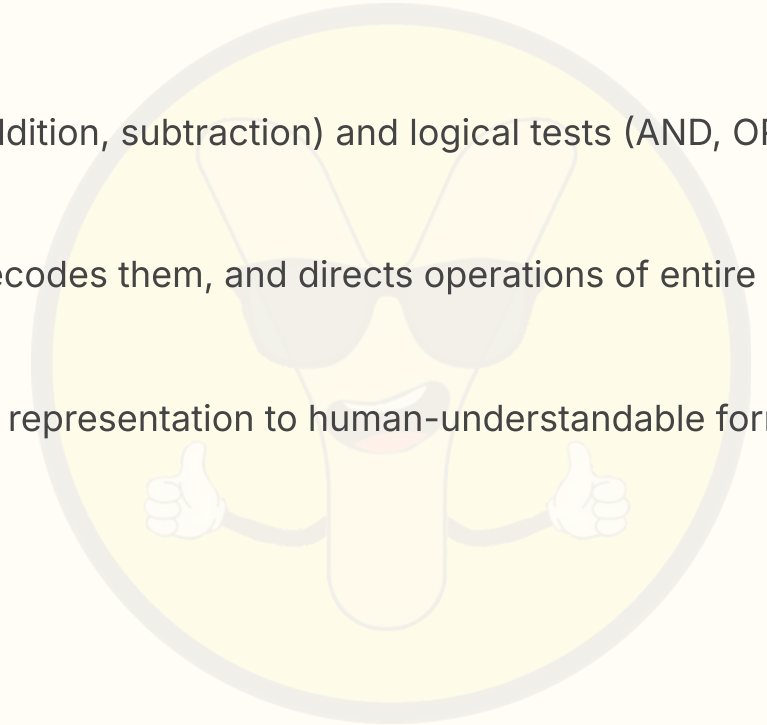
- Input Unit
  - Accepts raw data and instructions from external sources.
  - Converts human-readable data into binary machine-readable format.
- Memory Unit
  - Stores programs, intermediate results, and final output data.
  - Divided into primary (RAM, ROM) and secondary storage.



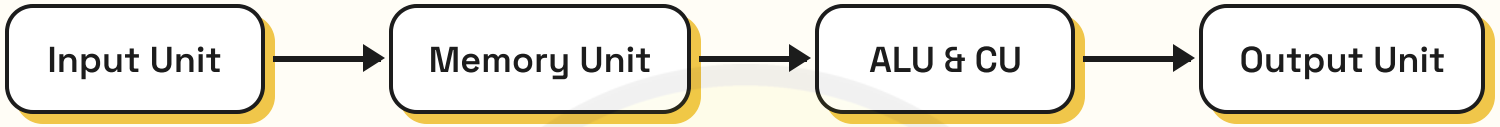
Functional Units: Processing and Output

Core execution and result delivery components.

- Arithmetic Logic Unit (ALU)
  - Performs mathematical operations (addition, subtraction) and logical tests (AND, OR, NOT).
- Control Unit (CU)
  - Extracts instructions from memory, decodes them, and directs operations of entire system.
- Output Unit
  - Translates binary results from internal representation to human-understandable format.



Interconnections of Functional Units



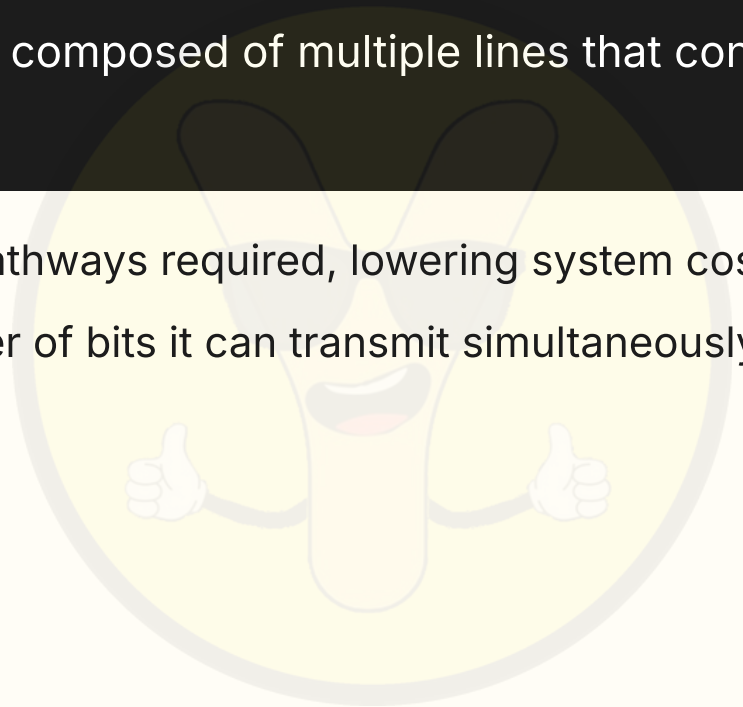
Data and control signal flow among major functional units of a digital system.

System Buses and Architecture

BUS

A shared communication pathway composed of multiple lines that connects two or more components of a computer.

- Reduces the number of separate pathways required, lowering system cost and complexity.
- Characterized by bus width (number of bits it can transmit simultaneously) and bus speed (clock frequency).



Types of System Buses

The system bus is categorized into three functional groups.

- Data Bus
  - Bi-directional lines used to transfer actual data between processor, memory, and I/O devices.
- Address Bus
  - Uni-directional lines used to specify the physical memory address or I/O port address for read/write operations.
- Control Bus
  - Mixed lines used to transmit command and timing signals (Memory Read, Memory Write, I/O Read, Interrupt).

Bus Arbitration

BUS ARBITRATION

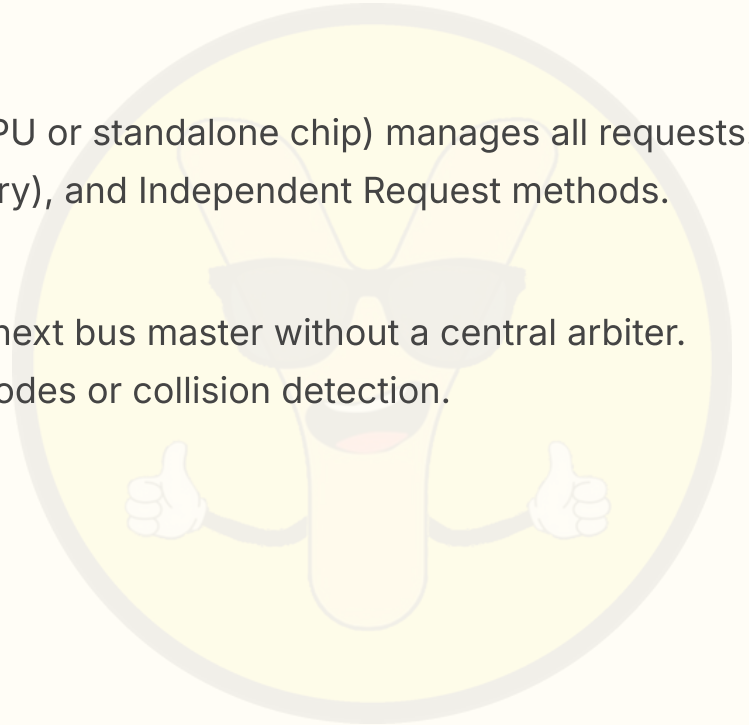
The process by which the current bus master accesses and relinquishes control of the system bus to prevent simultaneous access conflicts.

- Ensures only one device (processor or DMA controller) controls the bus at any given time.
- Classified broadly into centralized arbitration and distributed arbitration schemes.

Bus Arbitration Schemes

Techniques for managing shared bus access among multiple master devices.

- Centralized Arbitration
  - A single bus arbiter (often inside the CPU or standalone chip) manages all requests.
  - Includes Daisy Chaining, Polling (Enquiry), and Independent Request methods.
- Distributed Arbitration
  - All devices participate in selecting the next bus master without a central arbiter.
  - Uses self-selection based on priority codes or collision detection.

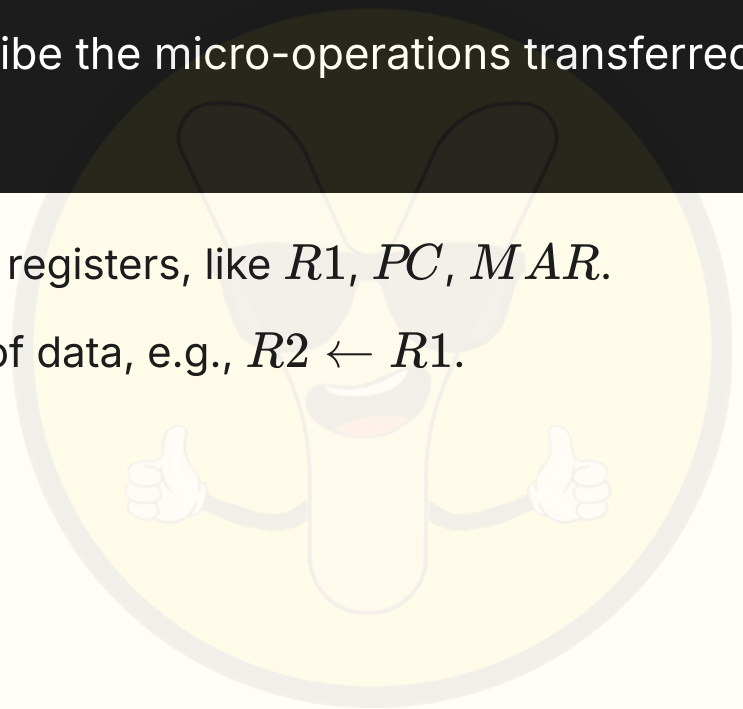


Register Transfer

REGISTER TRANSFER LANGUAGE (RTL)

A symbolic notation used to describe the micro-operations transferred among registers within a processor.

- Notation uses uppercase letters for registers, like $R1$, PC, MAR.
- Arrow symbol $\leftarrow$ denotes transfer of data, e.g., $R2 \leftarrow R1$.



Bus and Memory Transfers

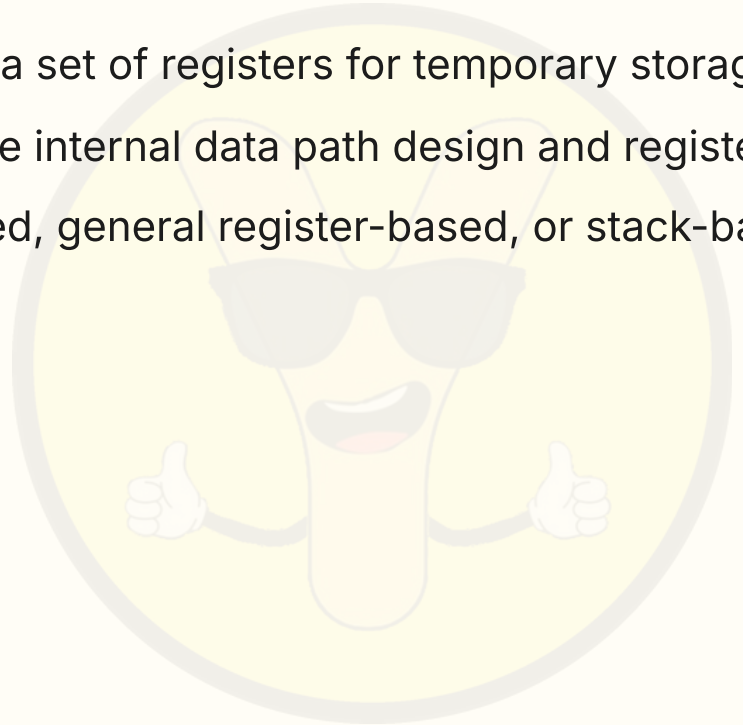
Mechanisms for moving data across common buses and to/from main memory.

- Common Bus System using Multiplexers
  - Multiplexers select which register output is placed onto the common bus lines.
- Three-State Bus Buffers
  - Alternative to multiplexers using gates with high-impedance (High-Z) states to isolate inactive outputs.
- Memory Transfer Operations
  - Read operation: $Data \leftarrow M[MAR]$; Write operation: $M[MAR] \leftarrow Data$.

Processor Organization Overview

Internal structural layout of the Central Processing Unit.

- Contains an ALU for computations, a set of registers for temporary storage, and a control unit.
- Organization depends heavily on the internal data path design and register availability.
- Designed around accumulator-based, general register-based, or stack-based architectures.



General Register Organization

CPU architecture featuring multiple general-purpose registers instead of a single accumulator.

- Register-Memory Architecture
  - Instructions can access operands from registers or main memory (e.g., x86).
- Register-Register (Load-Store) Architecture
  - Arithmetic operations occur strictly between registers; memory accessed only via Load/Store (e.g., ARM, MIPS).
- Advantages
  - Faster execution, reduced memory traffic, and greater compiler optimization potential.

Stack Organization

STACK

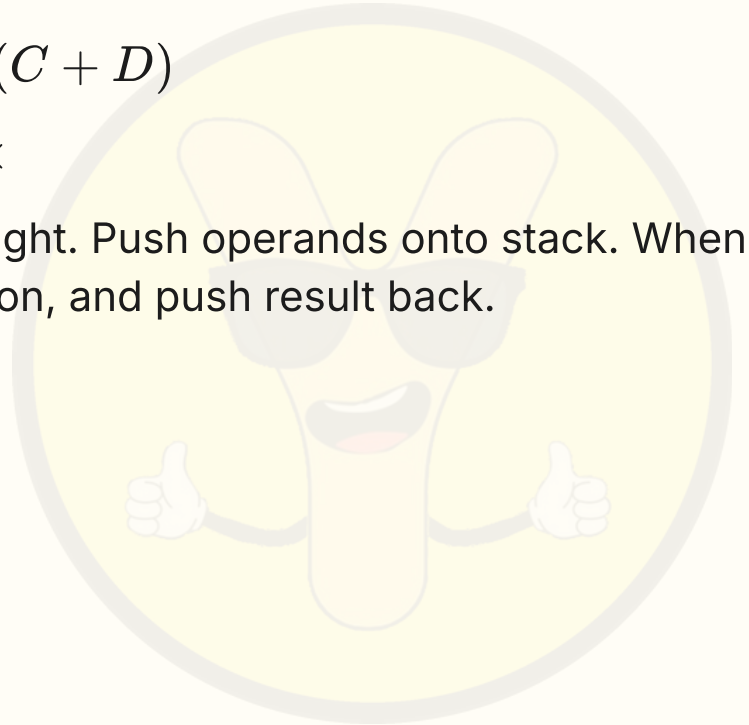
A Last-In-First-Out (LIFO) storage structure where items are added and removed from only one end called the top of the stack.

- Managed using a dedicated hardware register called the Stack Pointer (SP).
- Supports two primary operations: PUSH (adds item, decrements/increments SP) and POP (removes item, increments/decrements SP).

Evaluation of Expressions using Stack

Stack organization excels at processing arithmetic expressions in Reverse Polish Notation (Postfix).

- Infix expression: $X = (A + B) \times (C + D)$
- Postfix expression: $AB + CD + \times$
- Algorithm: Scan expression left to right. Push operands onto stack. When operator is encountered, pop required operands, perform operation, and push result back.

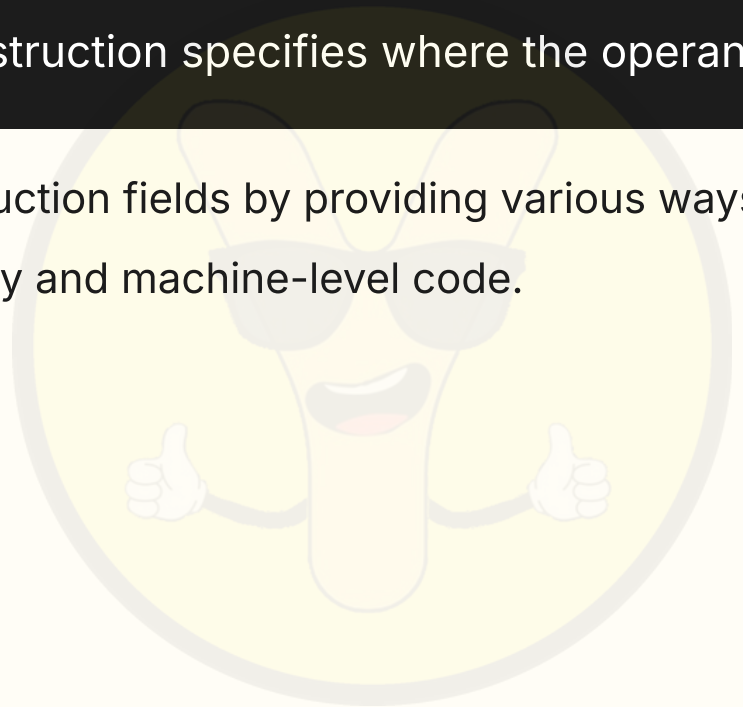


Introduction to Addressing Modes

ADDRESSING MODE

The rule or manner in which an instruction specifies where the operand for an operation is located.

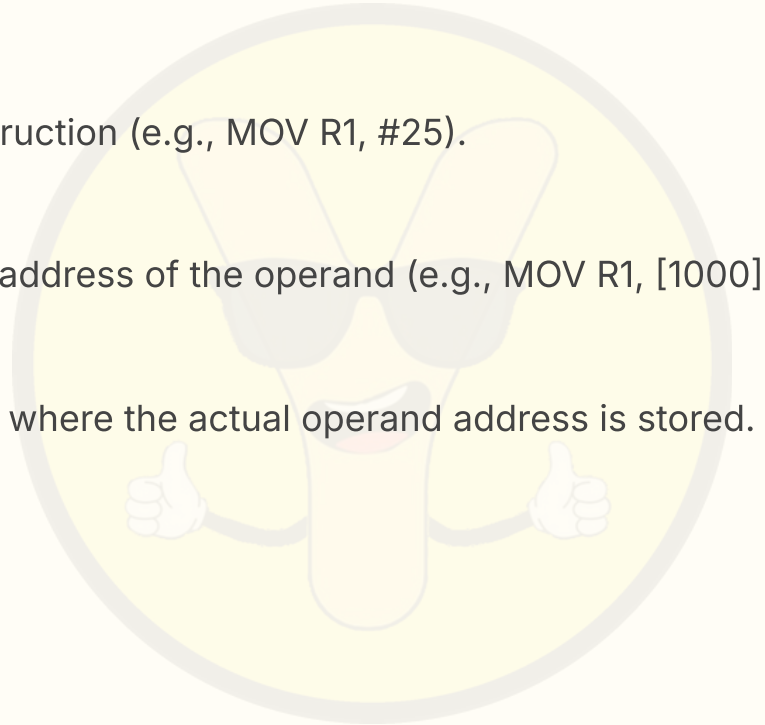
- Reduces the number of bits in instruction fields by providing various ways to calculate the effective address.
- Crucial for writing efficient assembly and machine-level code.



Common Addressing Modes

Standard modes implemented in most instruction set architectures.

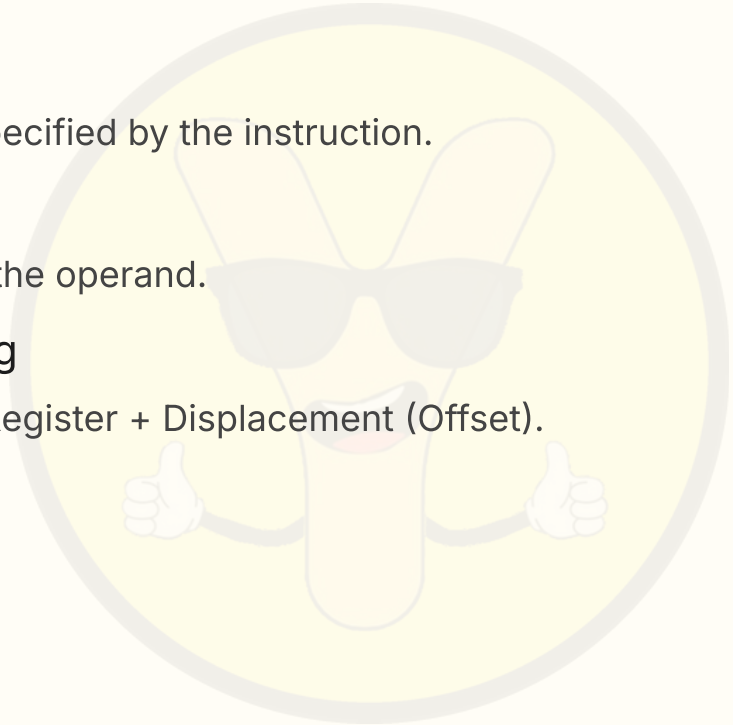
- Immediate Addressing
  - Operand is specified directly in the instruction (e.g., MOV R1, #25).
- Direct (Absolute) Addressing
  - Instruction contains the exact memory address of the operand (e.g., MOV R1, [1000]).
- Indirect Addressing
  - Instruction contains a memory address where the actual operand address is stored.



Advanced Addressing Modes

Modes utilized for arrays, loops, and position-independent code.

- Register Addressing
  - Operand is located in a CPU register specified by the instruction.
- Register Indirect Addressing
  - Register holds the memory address of the operand.
- Indexed & Base-Register Addressing
  - Effective Address = Contents of Base Register + Displacement (Offset).



Comparison of Key Addressing Modes

Addressing Mode	Operand Location	Speed	Flexibility
Immediate	Inside instruction	Fastest	Low (constant value)
Direct	Main memory	Slow	Medium
Register	CPU Register	Very Fast	Limited by register count
Indexed	Memory (Base + Offset)	Moderate	High (great for arrays)

Exam corner

Q1 Explain the functional units of a digital computer with a neat block diagram.

Q2 What is bus arbitration? Compare centralized and distributed bus arbitration techniques.

Q3 Explain common bus organization using multiplexers and three-state buffers.

Q4 Differentiate between general register organization and stack organization in CPUs.

Q5 Evaluate the arithmetic expression $X = \frac{A+B}{C \times D}$ using a zero-address stack computer.

Q6 Define addressing mode. Explain Direct, Indirect, Immediate, and Indexed addressing modes with examples.

Q7 Write short notes on Register Transfer Language (RTL) and memory read/write micro-operations.

Unit 1 done. You are exam-ready.

Revise the Exam corner once more, then open Unit 2 on theycotes.com. Every AKTU subject, unit by unit, free. Notes by Chirag Jain, Ycotes.

